

Notice of References Cited

Application/Control No.

10/760,621

Applicant(s)/Patent Under
Reexamination
WILCOX ET AL.

Examiner

Nghia M. Doan

Art Unit

2825

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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,502,648	03-1996	Kaplan, Jonathan T.	716/17
*	B	US-6,874,134	03-2005	Collin et al.	716/3
*	C	US-6,252,448	06-2001	Schober, Robert C.	327/259
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Wu et al., Clock-gating and Its Application to Low Power Design of Sequential Circuits, March 2000, IEEE, Vol. 47, Pages 415-419.
	V	Lang et al., Individual Flip Flop with Gated Clocks for Low Power Datapaths, June 1997, IEEE, Vol. 44, Pages 507-516.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.